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Design of Single-Architecture Universal Shift Register and Counter with Memory Unit using Full-Swing GDI D-Flip-Flops

[1] **Vayara Prasanna Lakshmi**, [2] **Balla Divya Tejaswi**, [3] **Cheekatla Chishma Lakshmi Anantha Hyma**, [4] **Podalada Ramya Sindhu**, [5] **Appari Ramya Sri**

[1]M. TECH, Associate Professor, Dept of E.C.E, BVCITS, Batlapalem, Amalapuram, AP

[2,3,4,5]B. Tech, Dept of E.C.E, BVCITS, Batlapalem, Amalapuram, AP

Abstract: This research presents a novel single-architecture universal shift register/counter with an integrated memory unit. A full swing gate diffusion input (GDI) flip-flop is designed and implemented in both a synchronous counter and a universal shift register. SRAMs are mostly utilized as cache memory due to their ability to retain data when the power is ON. Hence, a 4 × 4 SRAM-based on full swing gate diffusion input flip-flop is developed to act as a memory for the proposed single-architecture universal shift register / Counter with the memory unit. To enhance performance, a 4 × 4 SRAM based on the proposed GDI flip-flop is incorporated as the memory unit. The design aims to improve key performance metrics, including clock-to-Q delay, power-delay product, area, and static power consumption. Simulation results demonstrate a 25% reduction in clock-to-Q delay, 30% reduction in D-to-Q delay, 20.2% reduction in power-delay product, 14.9% reduction in area, and 28.6% reduction in static power consumption compared to conventional D-flip-flop designs. The proposed architecture is validated through simulations using Tanner EDA at 1.2 V operating conditions, confirming its efficiency and potential applicability in high-performance sequential circuits.

Keywords: Universal Shift Register, Counter Architecture, Memory Unit, Gate Diffusion Input, Full-Swing Logic, D Flip-Flop, Low-Power VLSI Design, Sequential Circuits, High-Speed Digital Circuits, Reduced Transistor Count, CMOS Technology, Digital System Design.

Introduction: There are several different types of advanced systems, but the most frequent basic component is a flip flop. As a result of Moore's Law, CMOS innovation techniques have shrunk in size, enabling designers to fit more transistors onto a single chip [1]. The greater the number of transistors, the greater the amount of energy lost as heat or radiation. One of the most significant difficulties of low-power plan strategies and methodologies is the rising temperature. Due to the increasing importance of practical frameworks and the need to decrease control utilization (and thus warm dispersion) in high-thickness VLSI circuits, rapid and inventive improvements have been made in low-control design. Flip-flops are one of the most ubiquitous and fundamental computer components (FFs) [2]. Particularly sophisticated strategies these days sometimes include large pipelining systems [3] and the heavy reliance on feature-rich modules like enroll record, move enroll, and first in first out [4]. About half of the clock framework's total control's power consumption is expected to come from the clock itself. For this reason, FFs use a lot of resources from the chip. Consider the coordinated circuit's dependability together minimal power consumption. Higher levels of trading raise the potential for persistent quality issues since more normal current is discharged [5]. Tablets and other portable computing platforms are replacing laptops. Because of the persistence of this trend and the lack of any obvious solution in the near future of batteries, low power issues need a lot more 15 | Page attention. Future integrated circuits' energy consumption patterns may be coordinated based on the current trends because of the computerization of low-power plans. To achieve low power consumption there are requirements to design and develop low power consumption devices. Due to the increment of portable system and rapid development in electronic sector a low power and less area and speed improved device is necessary to archives this goal. Therefore, the research goal of this paper is to propose a design of a low power, speed improved 4-bit universal shift register using D flip flops and multiplexers. Power consumption and area reduction of logic and memory have become primary focuses of attention in VLSI digital design [1–6].

Power is the limiting factor in both high performance systems and portable applications. Die area directly affects the device size and cost. Since the introduction of the standard CMOS Logic in early 80s, many design solutions have been proposed to improve power dissipation, area and performance of digital VLSI chips. Gate Diffusion Input (GDI) design methodology was introduced as a promising alternative to Static CMOS Logic [7]. Originally proposed for fabrication in Silicon on Insulator (SOI) and twin-well CMOS processes, GDI methodology allowed implementation of a wide range of complex logic functions using only two transistors [7]. It was shown, that area and dynamic power of GDI combinatorial and sequential logic were significantly reduced, as compared to standard CMOS implementations. Similarly to existing alternatives to CMOS, such as Pass Transistor Logic (PTL), the GDI gates presented reduced voltage swing at their outputs due to threshold drops. These drops usually cause degradation in performance and increased short circuit power [8]. However, since the GDI circuits were implemented with much less transistors, a significant power overall power reduction was observed, while maintaining minimal performance penalty Recently, it was shown that any GDI circuit can be implemented in a standard CMOS process [8].

LITERATURE REVIEW: Significant and new improvements in low-power design have emerged from the need for portable devices and the necessity to minimize power consumption in VLSI processors [6]. Battery life, speed, power consumption, and size all need to be optimized for small silicon areas in order to make portable devices viable. There is widespread usage of synchronous circuits in digital circuits because of their ability to reduce design complexity. Flip-flops are a crucial timing element in digital circuits [7], but they have a significant impact on the circuit's speed, size, and power consumption. The most recent data input signal is kept in the flip-flop when a clock signal is present. DFFs are a major source of the heat generated by VLSI systems. Recording of the value of the D input occurs once per clock cycle. Captured values are used to calculate the Q output. These flip-flops provide the basis of the shift registers used in many electrical devices. The D FF behaves like a D-type transparent latch in that it retains the status of the signal on its D input pin when it is clocked but ignores any changes made to that input until it is clocked again [6,7]. The research in this paper looked at both double-edge triggered flip-flops (DEFFs) and clocked pair sharing (CPSFF) flip-flops. Single-ended conditional energy recovery (SCCER) and double ended (DETFF) and triple- ended (CDMFF) flip-flops (MTCMOS) were also tested and rated. A PIPO shift register makes use of the studied flip flops. The two top flip-flops were chosen based on their power ratings. One may use a clock pulse sense latch in a number of different ways to create a 4-bit universal shift register [8]. In an irreversible circuit, if one bit information is lost then at least KTln2 joules of energy is dissipated. Where K is Boltzmann's constant and T is absolute temperature. This was stated by Landauer R in 1961[1]. In 1973, Bennett[2] proved that, KTln2 joules of energy dissipated due to information loss in irreversible circuit can be controlled by reversible logic where the reversible circuit allows to reproduce the inputs from output resulting in no information loss. He also showed that reversible systems can do the same computations as the classical or irreversible systems at same efficiency. This leads to the evolution of reversible logic based systems. Any reversible gate should have equal number of inputs and outputs such that, inputs can be recovered uniquely from outputs at any point of time. In paper [3], by Shibinu A.R , Rajkumar, a 4- bit LFSR design using Muller expression is proposed. This paper also gives realization of both edge triggered and level triggered D flip flop using reversible logic. At the end, comparative analysis has been given between conventional LFSR and Reversible LFSR. From this it is observed that, the proposed technique is efficient than conventional technique in implementing LFSR in terms of cost metrics like power, quantum cost, garbage output and gate count. D. Muthih and A. Arockia Bazil Raj [4] have presented a parallel architecture for designing high speed LFSR and explained that, BCH encoders and CRC operations are normally carried out by using LFSR. A novel approach for high speed BCH encoder is proposed. This paper presents two key points. First, it presents a linear transformation algorithm for converting a serial LFSR into parallel architecture, which can be used for generating polynomials in CRC and BCH encoders. Secondly, a new approach is proposed to amend parallel LFSR into pipelining and retiming algorithm. In paper [5], authors have presented two design approaches for designing reversible D FF with asynchronous set/reset which are optimized in terms of quantum cost, delay and garbage outputs. It also includes the design of 3 bit LFSR using two design approaches. The application of these FF's as LFSR is designed and discussed.

EXISTING METHOD:

CONVENTIONAL:

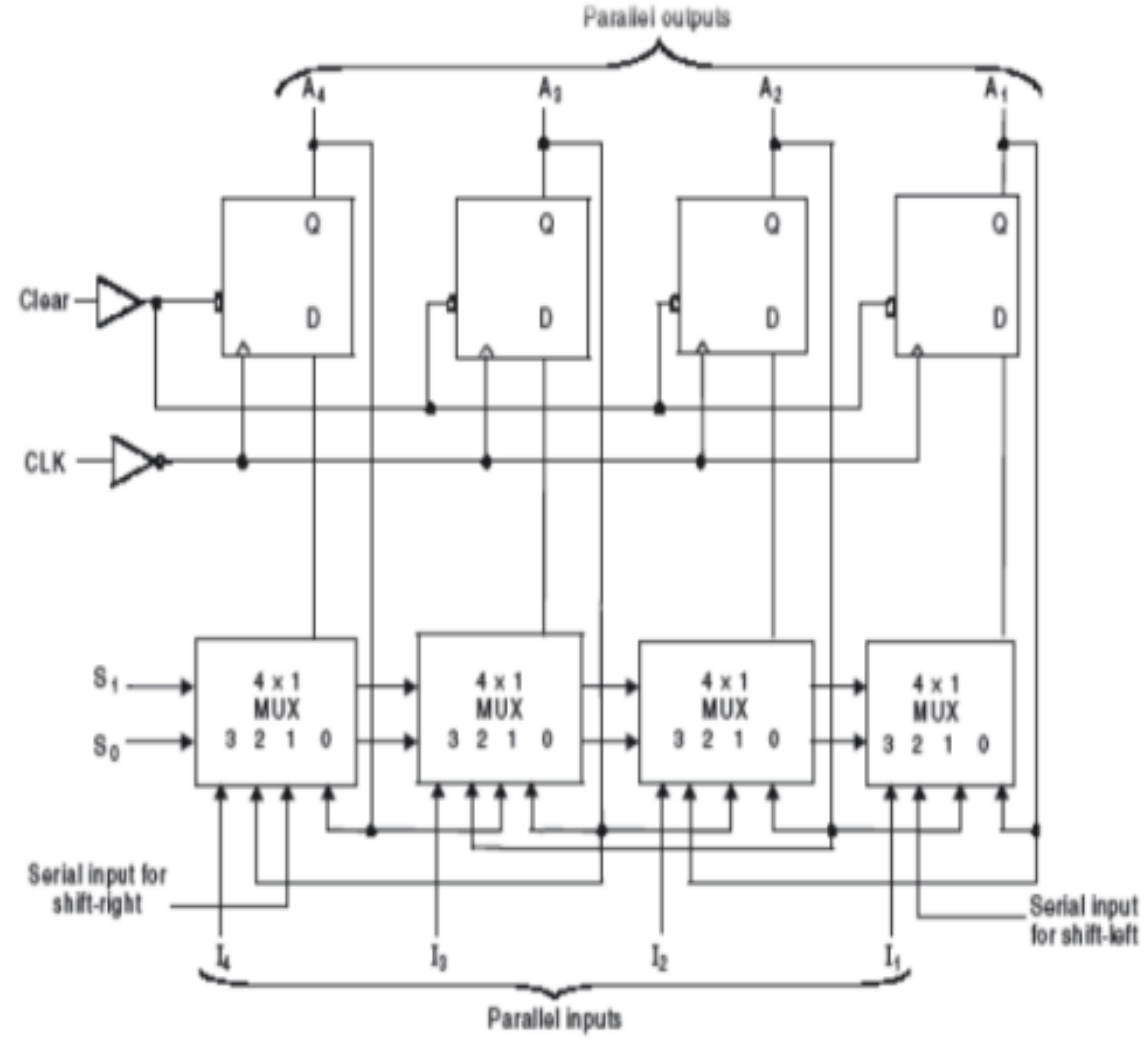

Fig1: schematic for a universal 4-bit shift register

This register's mode of operation is selected via the S0 and S1 pins. The parallel mode, the shift left operation, and the shift right operation are all viable alternatives.

- Pin 0 of the first 4x1 multiplexer is linked to the output of the first flip-flop. Please keep in mind the connections in this graphic.
- Shift-right serial input is connected to the first 4X1 MUX's Pin-1. Information is "right-shifted" by the register in this configuration.
- Like the serial input for shift-right, it is connected to pin-2 of the 4X1 MUX. The universal shift register moves all data one place to the left while in this mode.
- In order to facilitate parallel mode operation, the initial 4x1 MUX requires data to be fed to its third pin (I2), which then saves the information in a register. The third input pin of the 4X1MUX is used to load

the remaining data bits from the parallel input. The parallel outputs of the flip-flops connected to the 4x1 MUX are designated by the letters Q1, Q2, Q3, and Q4.

DFAL 4 BIT UNIVERSAL SHIFT REGISTER:

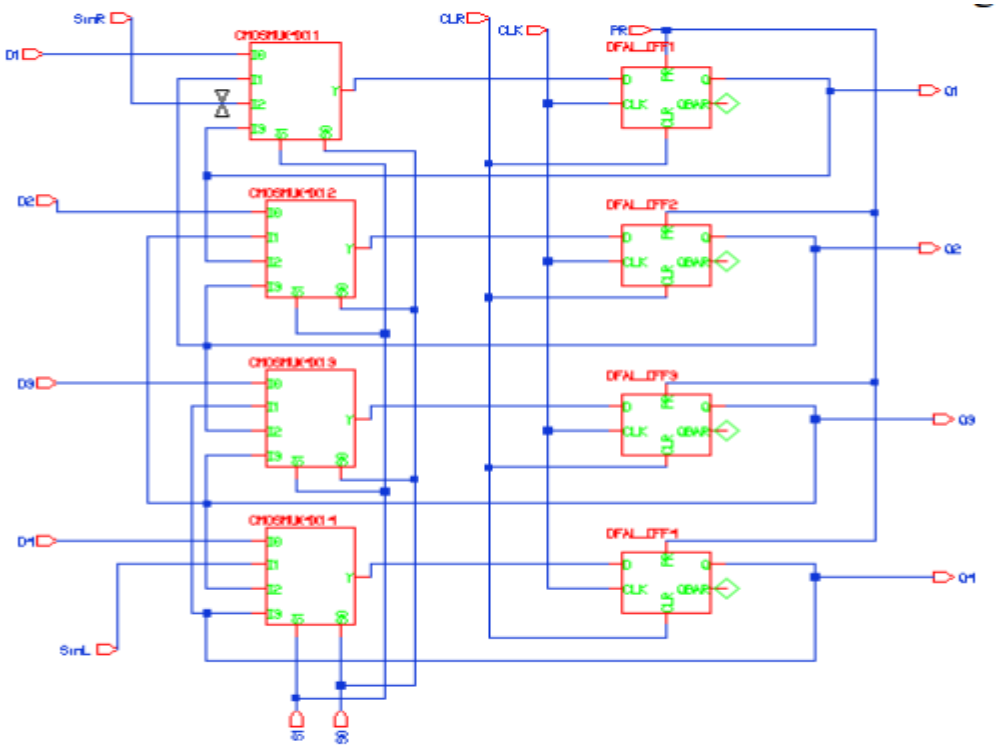

Fig. 2DFAL 4 Bit Universal Shift Register Schematic

As shown in above Figure, D1, D2, D3 and D4 are the parallel inputs and Q1, Q2, Q3 and Q4 are the parallel outputs. To shift the data both left and right, a serial input port is provided to input the corresponding data.

TABLE I. OPERATING MODES OF UNIVERSAL SHIFT REGISTER

S1	S0	Operating Mode
0	0	Parallel Load
0	1	Shift Left
1	0	Shift Right
1	1	Locked

Mode S1 = 0 and S0 = 0, correspond to the parallel loading of the universal shift register. When S1 = 0 and S0 = 1, then it is in the shift left mode. When S1 = 1 and S0 = 0 then it is in the shift right mode. When S1 = 1 and S0= 1, then the register results in locked mode, which means implies no operation. Time delays in various digital circuits are provided by the serial in serial out shift registers. Whereas serial in parallel out registers are used for serial to parallel transformation of the data. Similarly parallel in serial out

registers are used for parallel to serial transformation of the data. Shift registers are used in computers as memory elements. A large amount of data has to be stored in all types of digital circuits and systems that too in an efficient manner so; there is the need to use storage components like RAM and different registers.

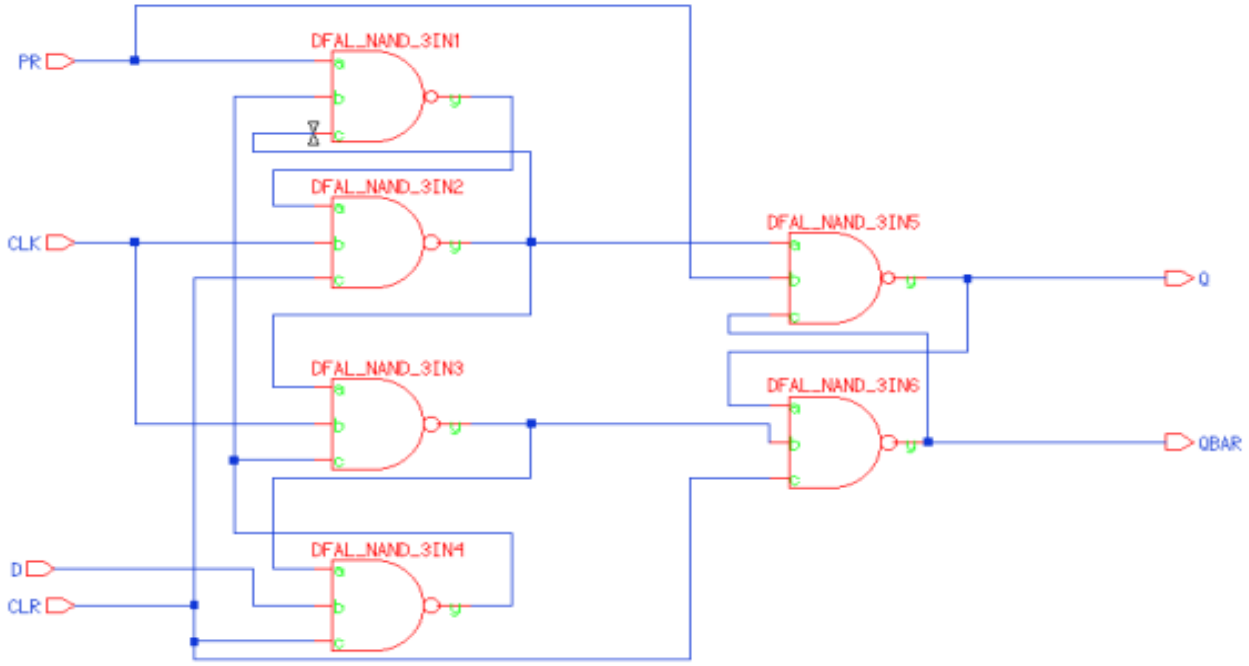

Fig. 3 DFAL D flip flop Schematic

The DFAL D Flip Flop is designed as shown in above figure.

PROPOSED METHOD:

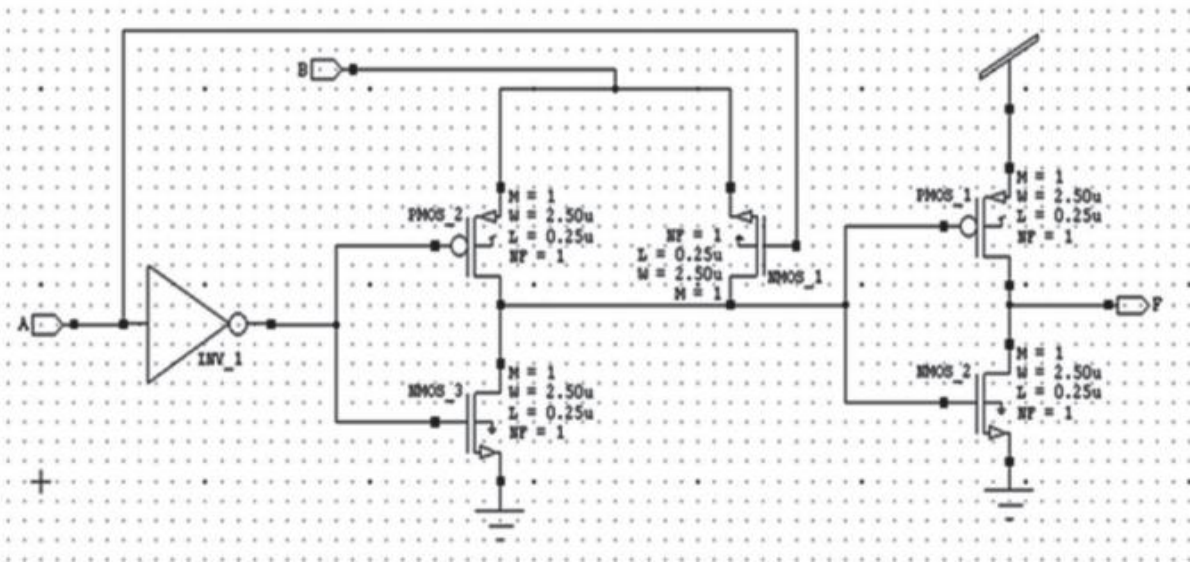

Figure 4: 2 Input FSGDI NAND primitive

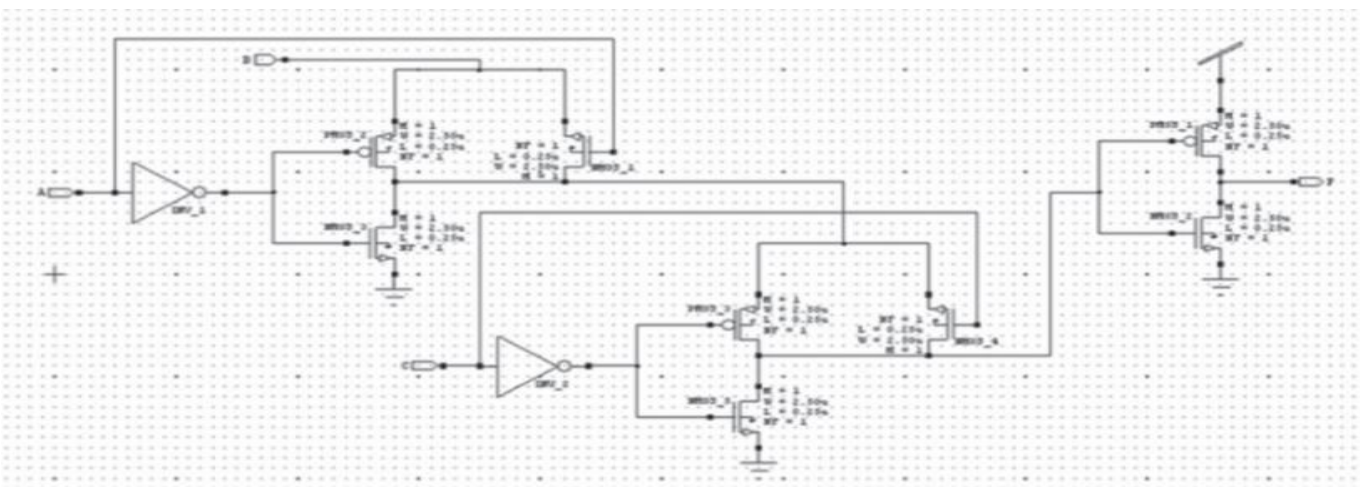

Figure 5: 3 Input FSGDI NAND primitive

D-flip-flop. The Output waveform of FSGDI PETD FlipFlop is shown in Figure 4. The conventional design is also simulated using tanner EDA and the schematic is shown in Figure.

FOUR-BIT UNIVERSAL SHIFT REGISTER AND COUNTER USING FSGDI PETD FLIP-FLOPS:

A logic circuit that has three unique modes for moving information is called a universal shift register. Figure 6 shows how a four-bit universal shift register is built using FSGDI-based Positive Edge set off D flip failures. Figures 7 and 8 each illustrate the waveforms of the right shift and left shift activity independently.

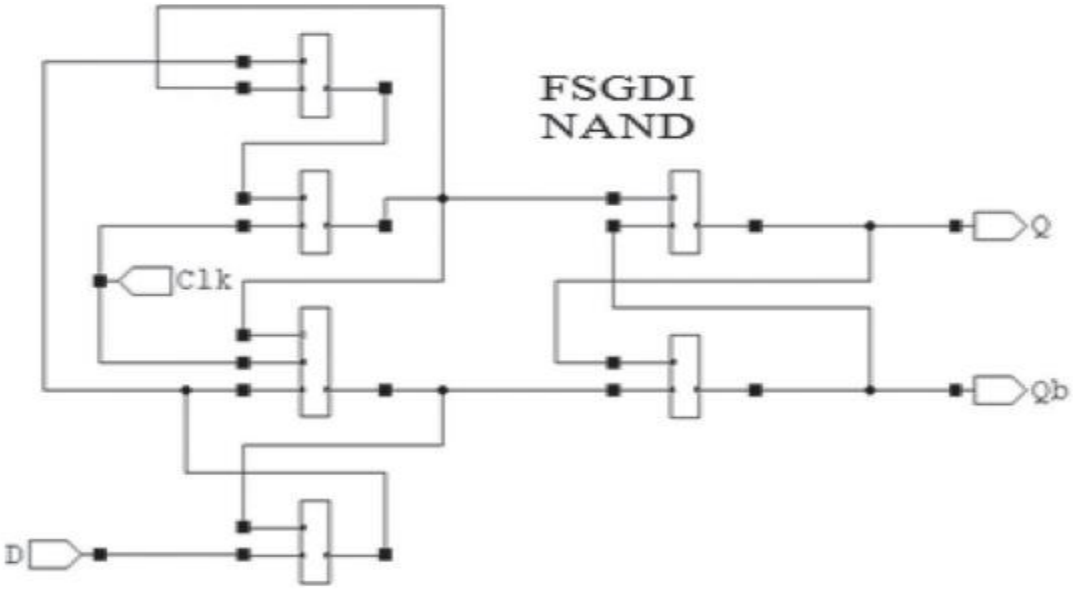

Figure 6: FSGDI-based positive-edge-triggered D flip-flop

It can stack and send information simultaneously, much like an equal register. It can stack and send information sequentially by left or right moves, just like shift registers do. Similar to the equal and sequential shift registers, the all-inclusive shift register combines their capacities. A broad catalog can transmit yield information in analogous and stack information in the chain on a single work. A counter is a structure that stores the amount of times a particular incident or process has happened, often in bond to a clock signal as discussed in the previous chapter. The use of full swing gates makes the design produce full swing output voltage with reduced power consumption.

PROPOSED DESIGN OF SINGLE-ARCHITECTURE UNIVERSAL SHIFT REGISTER AND COUNTER WITH MEMORY UNIT USING FSGDI D-FLIP-FLOPS :

The design of SRAM usually involves edge-triggered flipflops. The merits of using edge-triggered flip-flops are more. The 4 × 4 SRAM using edge-triggered D-flip-flop is shown in Figure 11. The design consumes 16-edge-triggered flip-flops that form the basic building block of this SRAM cell. The structure contains decoder circuitry, logic gates, and tristate buffers. The CS represents chip select, which indicates there is no operation when it is low and previous data is maintained in the memory cell as long as power is ON. The READ and WRITE operation using an example set of inputs is given in Table. The READ and WRITE operation is unwavering by the status of the RD signal. WRITE operation is performed when RD is low and READ operation is performed when RD is high. The A1 and A0 signal determines the respective word 0 to word 3. OE represents output enable which is to be maintained high for READ operation. The structure of 4 × 4 SRAM using FSGDI-based PETD is shown in Figure 12 and simulation values are given in Table. The proposed architecture combines both a universal shift register and synchronous counter by using the same set of edge-triggered D-flip-flops for its operation as shown in Figure 13. The design involves individual combinational logic blocks, multiplexers, edge-triggered D-flip-flops, and 4 × 4 SRAM as its memory unit. A single-architecture universal shift register and counter with a memory unit is designed based on FSGDI flip-flops. The operation of the single-architecture universal shift register and counter with memory unit is tabulated in Table. Static power consumption, primarily due to leakage currents, occurs even when the circuit is not switching. This includes subthreshold leakage, gate oxide leakage, and junction leakage.

Operation	CS	RD	OE	A1	A0	I3	I2	I1	I0	O3	O2	O1	O0
No operation	0	X	X	X	X	X	X	X	X	X	X	X	X
WRITE operation	1	0	X	0	0	0	0	0	1	X	X	X	X
	1	0	X	0	1	0	0	1	0	X	X	X	X
	1	0	X	1	0	0	1	0	0	X	X	X	X
	1	0	X	1	1	1	0	0	0	X	X	X	X
READ operation	1	1	1	0	0	X	X	X	X	0	0	0	1
	1	1	1	0	1	X	X	X	X	0	0	1	0
	1	1	1	1	0	X	X	X	X	0	1	0	0
	1	1	1	1	1	X	X	X	X	1	0	0	0

Table Operation of 4 × 4 SRAM using edge triggered flip-flop

Operation	C″/USR	En	S1	S0	ID	IC	IB	IA	QD	QC	QB	QA
COUNTER	0	0	X	X	X	X	X	X	X	X	X	X
	1	1	X	X	X	X	X	X	0	0	0	0
	1	1	X	X	X	X	X	X	0	0	0	1
	1	1	X	X	X	X	X	X	0	0	1	0
	1	1	X	X	X	X	X	X	0	0	1	1
USR – NO OPERATION	1	X	0	0	X	X	X	X	0	0	1	1
USR – RIGHT SHIFT	1	X	0	1	X	X	X	X	0	0	0	1
USR – LEFT SHIFT	1	X	1	0	X	X	X	X	0	0	1	0
USR – PARALLEL LOAD	1	X	1	1	1	0	0	1	1	0	0	1

Table: Operation of the single-architecture universal shift register and counter with memory unit

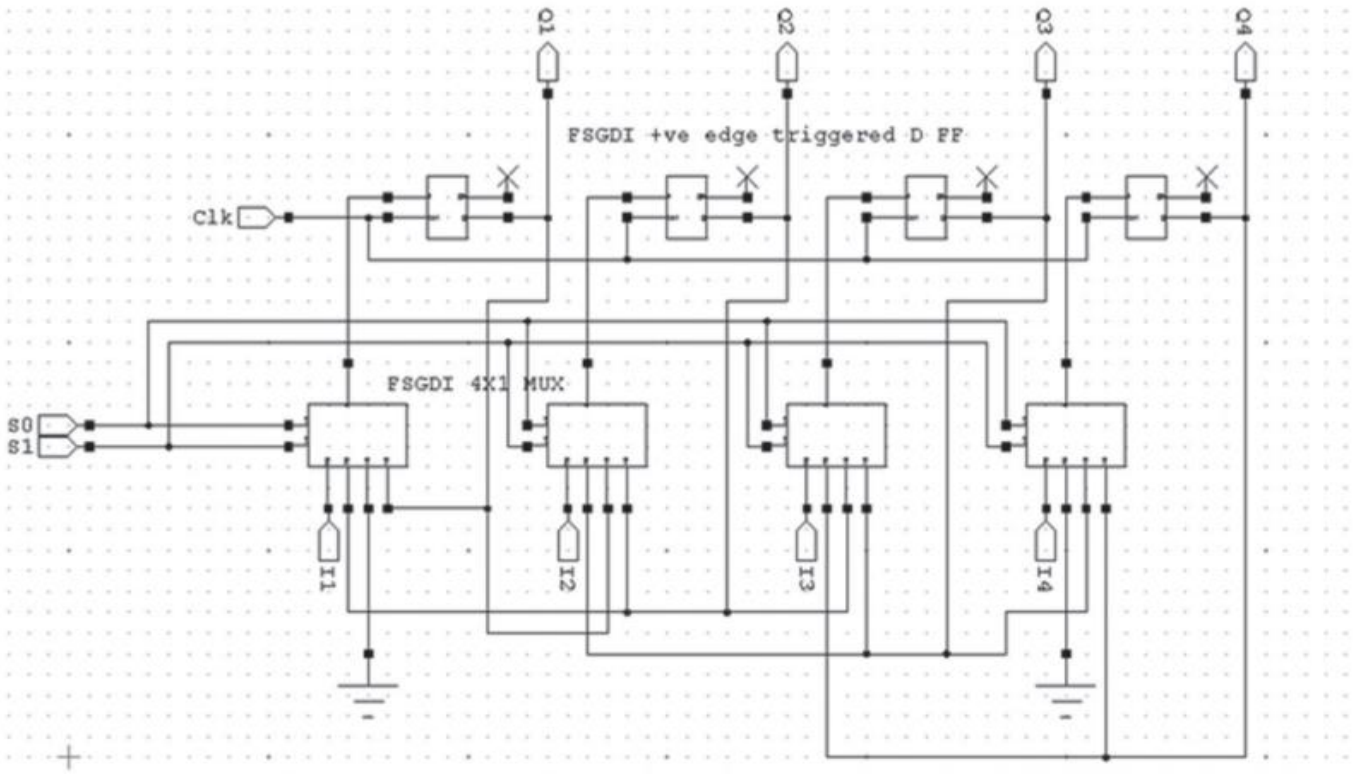

Figure 7: FSGDI-based 4-bit universal shift register using PETD FSGDI D flip-flop

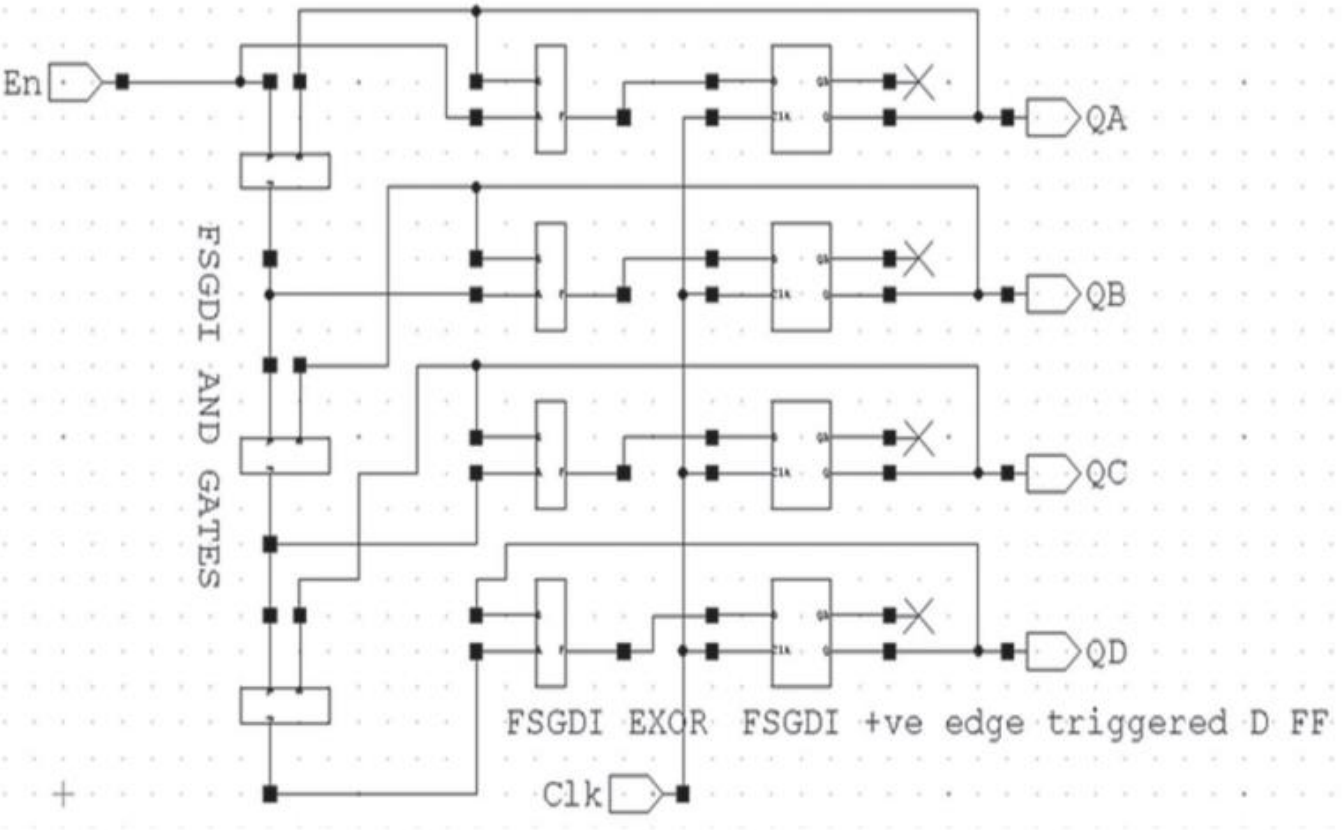

Figure 8 FSGDI-based 4-bit modulo synchronous counter using PETD flip-flop

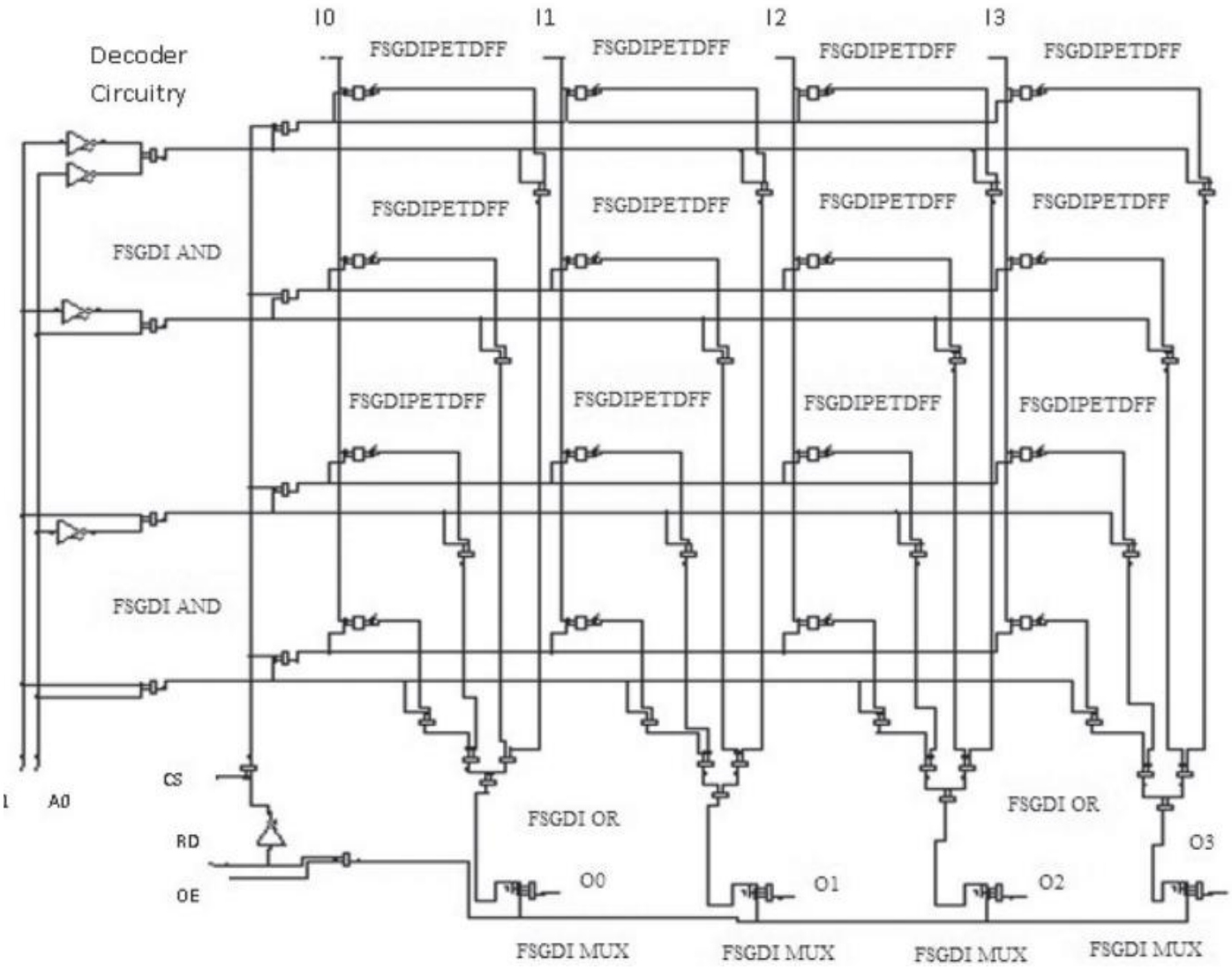

Figure 9: Structure of 4 × 4 SRAM using FSGDI-based edge-triggered D-flip-flops

Full Swing GDI (FS-GDI) Technique

The Gate Diffusion Input (GDI) technique is a digital circuit design methodology used in Very Large Scale Integration (VLSI) systems to reduce power consumption, transistor count, and propagation delay. Although GDI provides significant advantages over traditional CMOS Logic, it suffers from reduced voltage swing, which affects reliability and noise margins. To overcome this drawback, the Full Swing GDI (FS-GDI) technique was developed. FS-GDI modifies the conventional GDI structure to ensure full voltage swing at the output, improving performance and signal integrity.

In FS-GDI:

1. The main GDI structure performs the logic operation.
2. Additional transistors monitor the output.
3. If the output is degraded, the restoring transistor pulls it to:
    - **VDD** for logic HIGH
    - **GND** for logic LOW

Thus, the output achieves **full swing voltage levels**.

RESULTS:

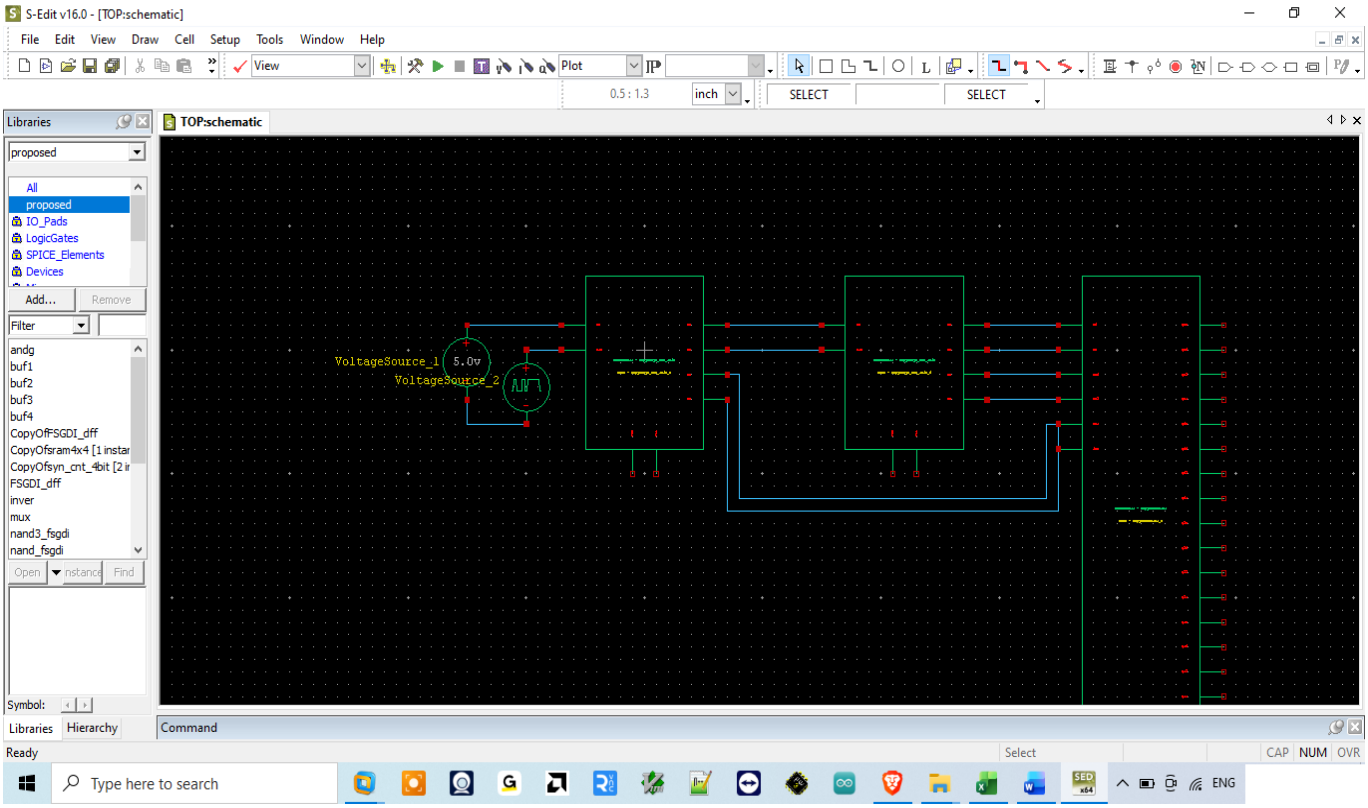

Fig: a Top level schematic

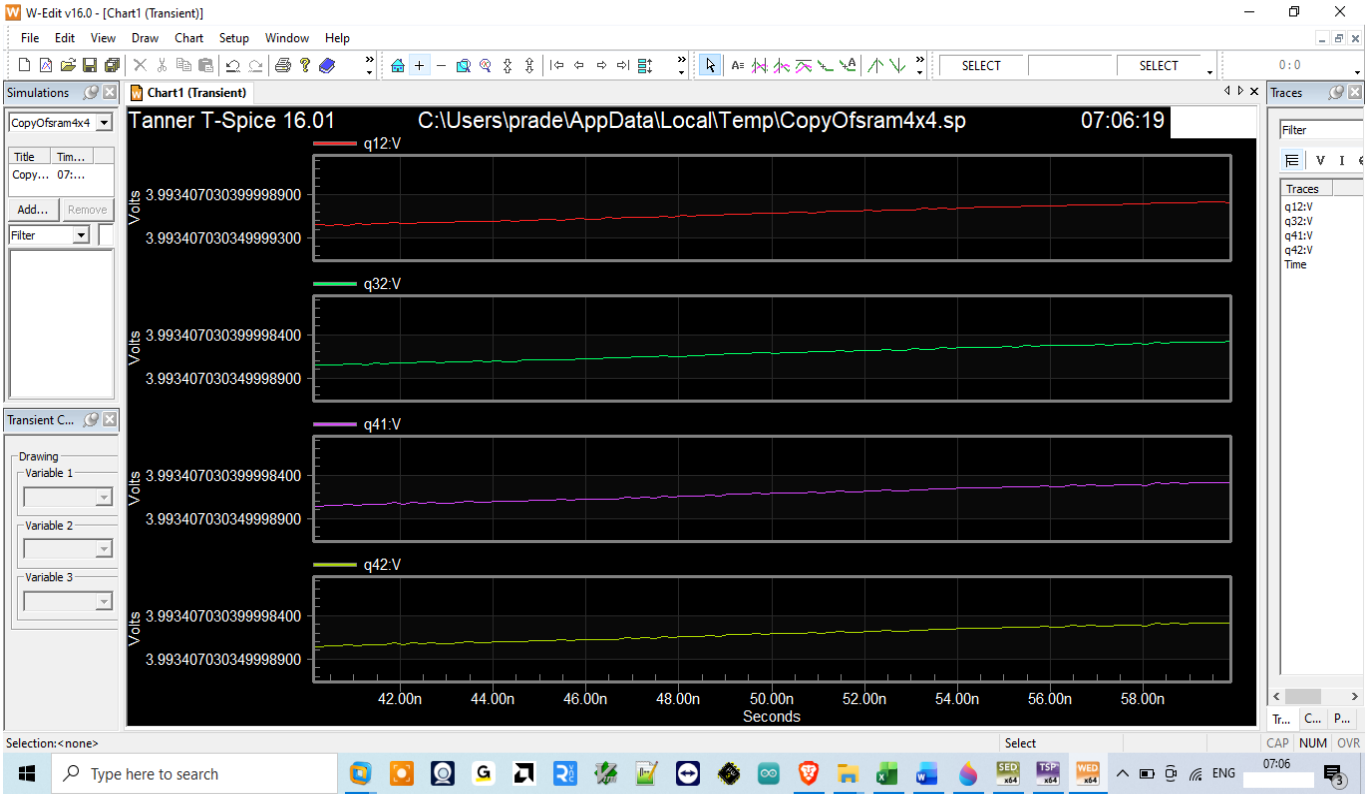

Fig: b Simulation results

Advantages

1. Low Power Consumption
   Using Gate Diffusion Input reduces switching power and leakage power compared to traditional CMOS circuits.
2. Reduced Transistor Count
   GDI logic requires fewer transistors to implement digital functions, which decreases circuit complexity.
3. High Speed Operation
   The design provides faster switching and reduced propagation delay, improving overall circuit performance.
4. Full Voltage Swing Output
   The D Flip-Flop implemented using full-swing GDI ensures proper logic levels, improving signal reliability.
5. Area Efficient Design
   The single architecture integrates shift register, counter, and memory unit, reducing chip area.
6. Multi-Functional Capability
   The universal shift register can perform multiple operations such as hold, shift left, shift right, and parallel load within the same circuit.
7. Improved Energy Efficiency
   Suitable for modern low-power VLSI systems where energy optimization is critical.

Applications

1. Digital Signal Processing Systems
   Used for data shifting, temporary storage, and serial-to-parallel data conversion.
2. Communication Systems
   Shift registers are used in data transmission and data synchronization.
3. Embedded Systems
   Useful in microcontrollers and processors for data manipulation and buffering.
4. Memory Devices
   Acts as temporary storage in digital circuits.
5. Counters and Sequence Generators
   Used in digital counters, timers, and sequence detection circuits.
6. Data Conversion Systems
   Used in serial-to-parallel and parallel-to-serial data conversion.
7. Low-Power VLSI Applications
   Suitable for portable electronic devices where power efficiency is essential.

Conclusion

The proposed design of a Single-Architecture Universal Shift Register and Counter with Memory Unit using Full-Swing GDI D-Flip-Flops presents an efficient approach for implementing multifunctional sequential circuits. By utilizing the Gate Diffusion Input, the circuit achieves reduced transistor count, lower power consumption, and improved operational speed compared to conventional CMOS-based designs. The integration of shift register, counter, and memory unit within a single architecture simplifies the overall hardware complexity and enhances area efficiency. The use of D Flip-Flop implemented with full-swing GDI logic ensures reliable signal levels and stable operation. Therefore, the proposed architecture provides a compact, power-efficient, and high-performance solution suitable for modern digital and VLSI systems.

Future Scope

1. The design can be extended to higher-bit architectures to support more complex digital systems and large-scale data processing.
2. Further optimization can be performed to achieve ultra-low power consumption for portable and battery-

operated devices.

3. The architecture can be implemented using advanced semiconductor technologies such as FinFET technology to improve speed and reduce leakage power.
4. Integration with other digital modules such as arithmetic logic units (ALUs) can enhance its application in processors and embedded systems.
5. The proposed design can be applied in low-power VLSI circuits, communication systems, and high-speed digital signal processing applications.
6. Future research may also explore hardware security and fault-tolerant designs to improve reliability in critical digital systems.

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